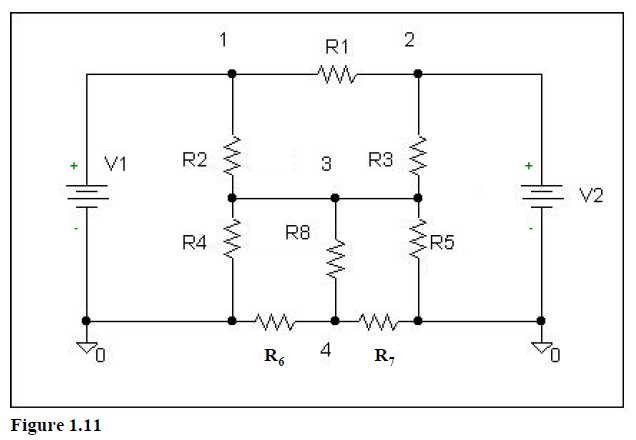
**1.10 Lab exercises**

**Exercise 1)**

1. Calculate (by hand) the voltages at all the nodes and the current through resistors R3, R4, and R5 in figure 1.11. R1=2k, R2=500, R3=2k, R4=1.5k, R5=1k, R6=10k, R7=2.2k, R8=200, V1=3.3V, V2=5V.
2. Show hand calculations.
3. Verify your results with HSPICE.
4. Print out node voltages from the output file. Compare them to the hand calculations.



The best way to solve this is to do a KCL at nodes 3 and 4:

\*

\*\*

From \*\*🡪  🡪 V3=1.111V4

Then from \*🡪 🡪 V3=1.95V, V4=1.755

Then, IR3, IR4, and IR5 are simple to find.

**\*\*\*\*\*\* operating point information tnom= 25.000 temp= 25.000 \*\*\*\*\***

**\*\*\*\*\* operating point status is all simulation time is 0.**

**node = voltage node = voltage node = voltage**

**+0:1 = 3.3000 0:2 = 5.0000 0:3 = 1.9503**

**+0:4 = 1.7556**

**\*\*\*\* resistors**

**subckt**

**element 0:r3 0:r4 0:r5**

**r value 2.0000k 1.5000k 1.0000k**

**v drop 3.0497 1.9503 1.9503**

**current 1.5248m 1.3002m 1.9503m**

**power 4.6502m 2.5359m 3.8038m**

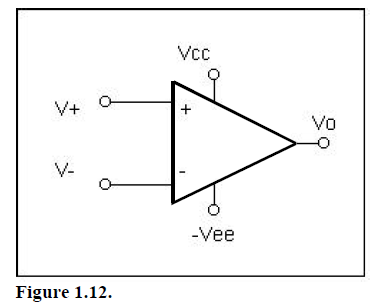
**Exercise 2)**

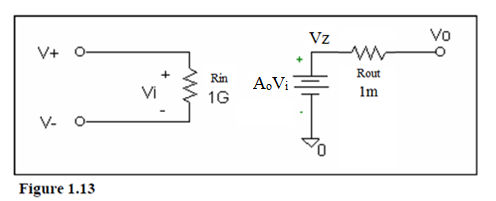
Figure 1.12 is a regular 741 op-amp. An op-amp can be modeled in SPICE by using the equivalent circuitry found in Figure 1.13.

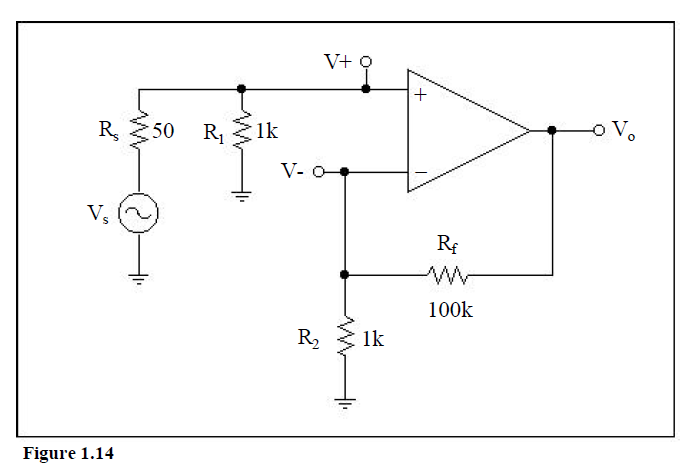
1. Compute the gain in figure 1.14 (by hand). Find the gain symbolically (do not use resistor values). Assume ideal op-amp impedances but not ideal gain (Rin=∞, Ao=Ao, Rout=0).
2. If we want maximum voltage transfer to the input of the op-amp, should R1>>Rs or should R1<<Rs? Why? For the rest of the problem, assume maximum voltage transfer.
3. What is the limit of the gain as Ao🡪∞? Let’s call this the **ideal gain**, or **Ai**.
4. Using your results in part 2, modify your gain equation to be in terms of only Ai, and A0.
5. What is the limit of the gain as Ao>>Ai? How much larger than Ai should Ao be for the gain to be within 1% of Ai? This exercise should give us an idea of either the lower limit of the gain of an op-amp (Ao) for a particular ideal gain, or the upper limit of the ideal gain for a particular op-amp gain (Ao).
6. Given the circuit resistor values in figure 1.14, find:
7. The ideal gain of the circuit (Ai).
8. The actual gain of the circuit if Ao=Ai, 10Ai, and 100Ai.
9. Use the equivalent circuit (figure 1.13) and HSPICE to verify your answers you found in part (B). Using a .TRAN analysis, let Vs be a SIN source with amplitude of 50mV and a frequency of 500Hz. Use the .*opt post* option and WaveView Analyzer for your plots.
10. What should tstep be if we want 1000 points/period?
11. What should tstop be if we want to plot 2 periods?
12. Simulate for Ao=Ai. Plot Vo and Vs on the same panel and attach a curser to verify the gain calculated in part B.
13. Repeat for Ao=10Ai and Ao=100Ai.
14. It should be noted that as Ao🡪∞, the two input nodes approach the same value. Repeat the simulation from part (C) but this time plot each input node of the op-amp. Note the changes when Ao goes from Ai to 100\*Ai.
15. Now, do not let Rout=0, but let Ao🡪∞ (as we just saw, this implies each input node to the op-amp are at the same voltage). Find the following gains in figure 1.14 (by hand) symbolically:
16. Vz/Vo.
17. If Rout~(R2+Rf), what is Vz/Vo?
18. If Rout>>(R2+Rf), what is Vz/Vo?
19. Given the circuit resistor values in figure 1.14, find:
20. R2+Rf. Let’s call this Rseen.
21. Vo/Vz if Rout=Rseen/100.
22. Vo/Vz if Rout=Rseen.
23. Use the same HSPICE simulation stimulus as in part C with Ao=100\*Ai. However, NOW WE WILL ADD +/- RAILS! Let the value of the +/- rails be +/-9V. (See page 11.)

1. Simulate for Rout=Rseen/100. Plot Vo, Vz, and Vs on the same panel. Attach a curser to verify the gains. Given the gains and input amplitude, explain why clipping occurs if it does.
2. Simulate for Rout=Rseen. Plot Vo, Vz, and Vs on the same panel. Attach a curser to verify the gains. Given the gains and input amplitude, explain why clipping occurs if it does.

Hopefully now you see why we want Rout of an op-amp to be much smaller than Rseen!





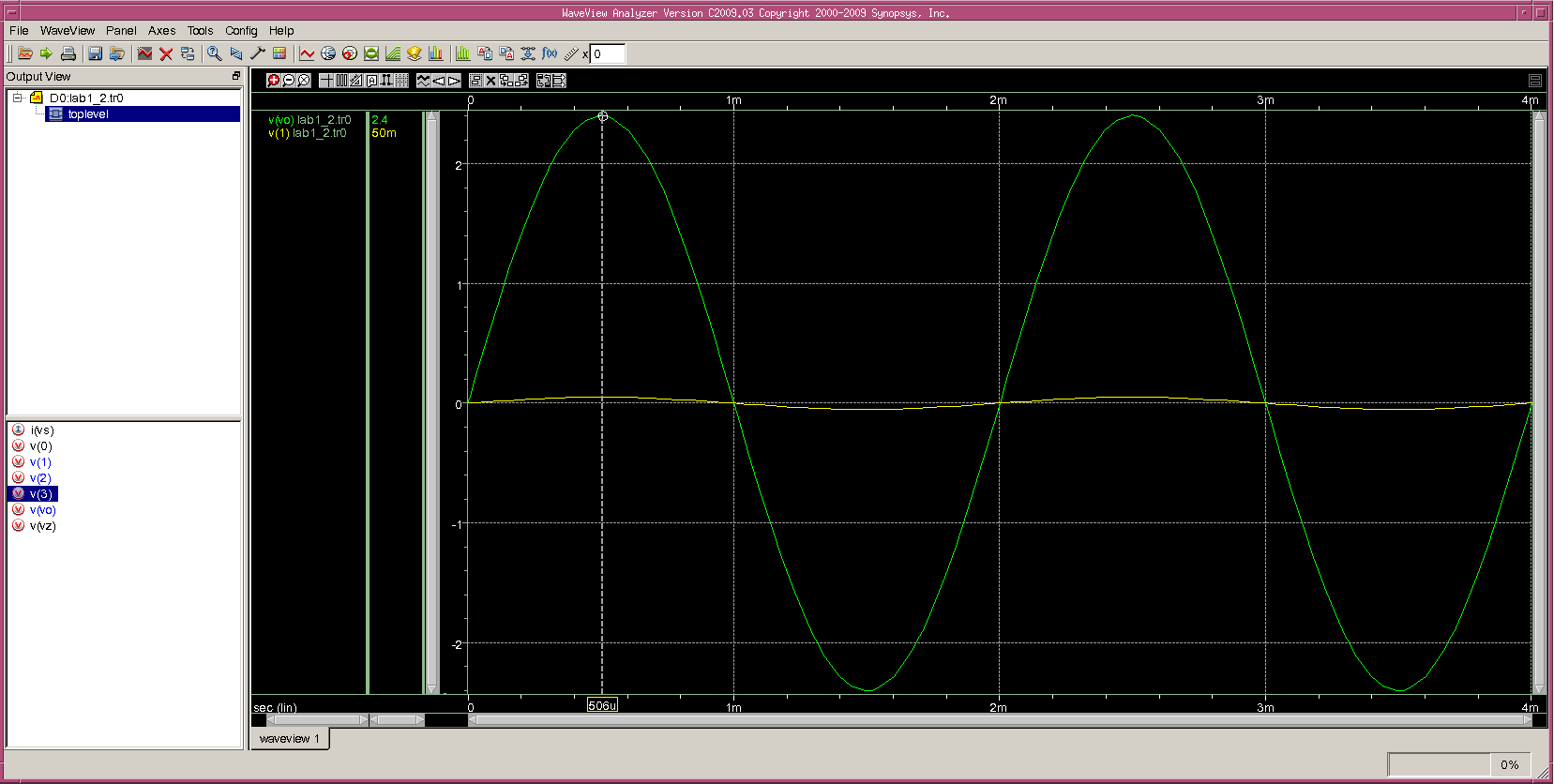




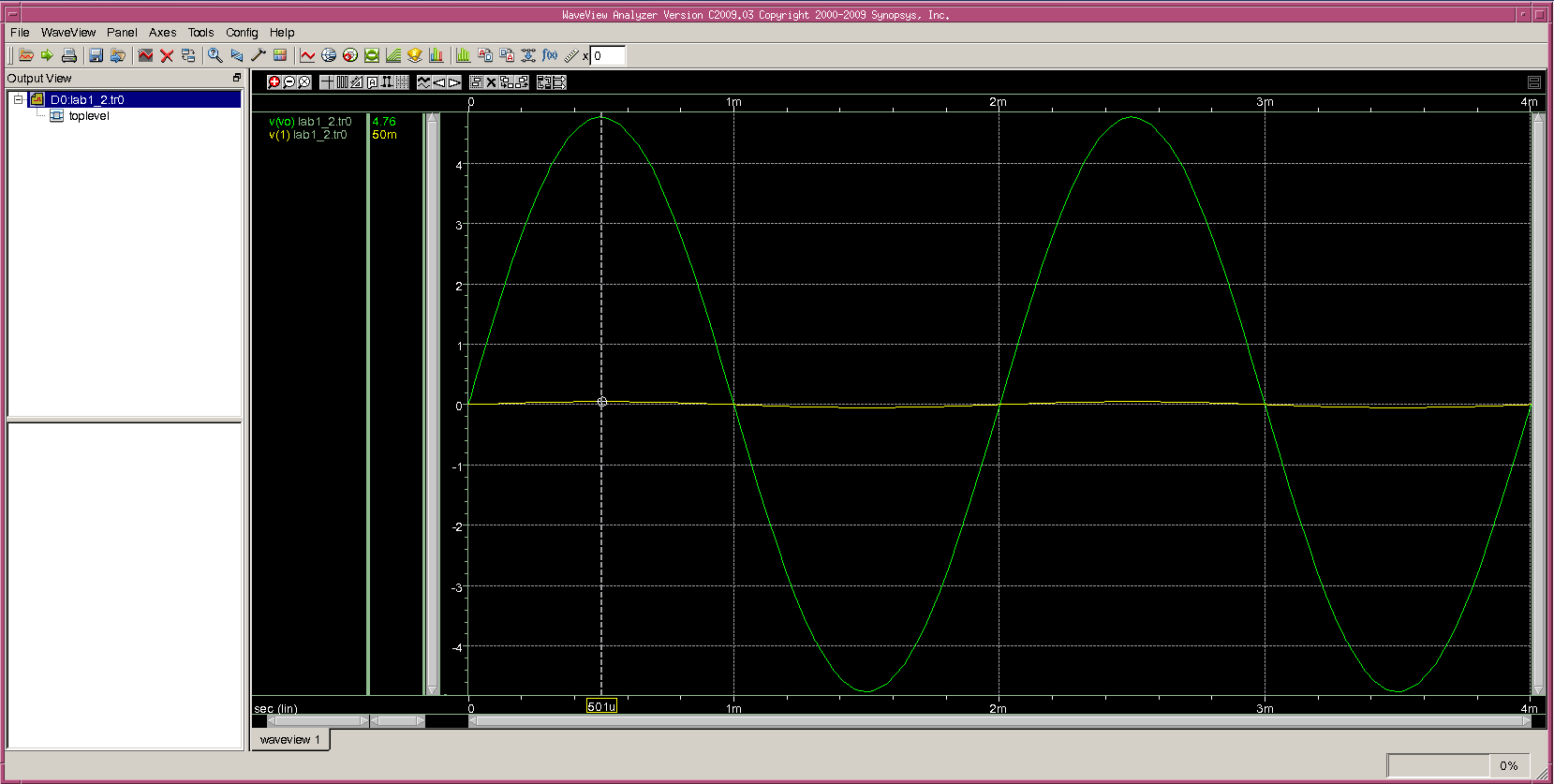
1. R1>>Rs because 
2. 
3. 
4. ~ Ao should be at least 99\*Ai to be within 1%.
5. 101. 48.095
6. 10,100. 95.24
7. 96.19

tstep=2us

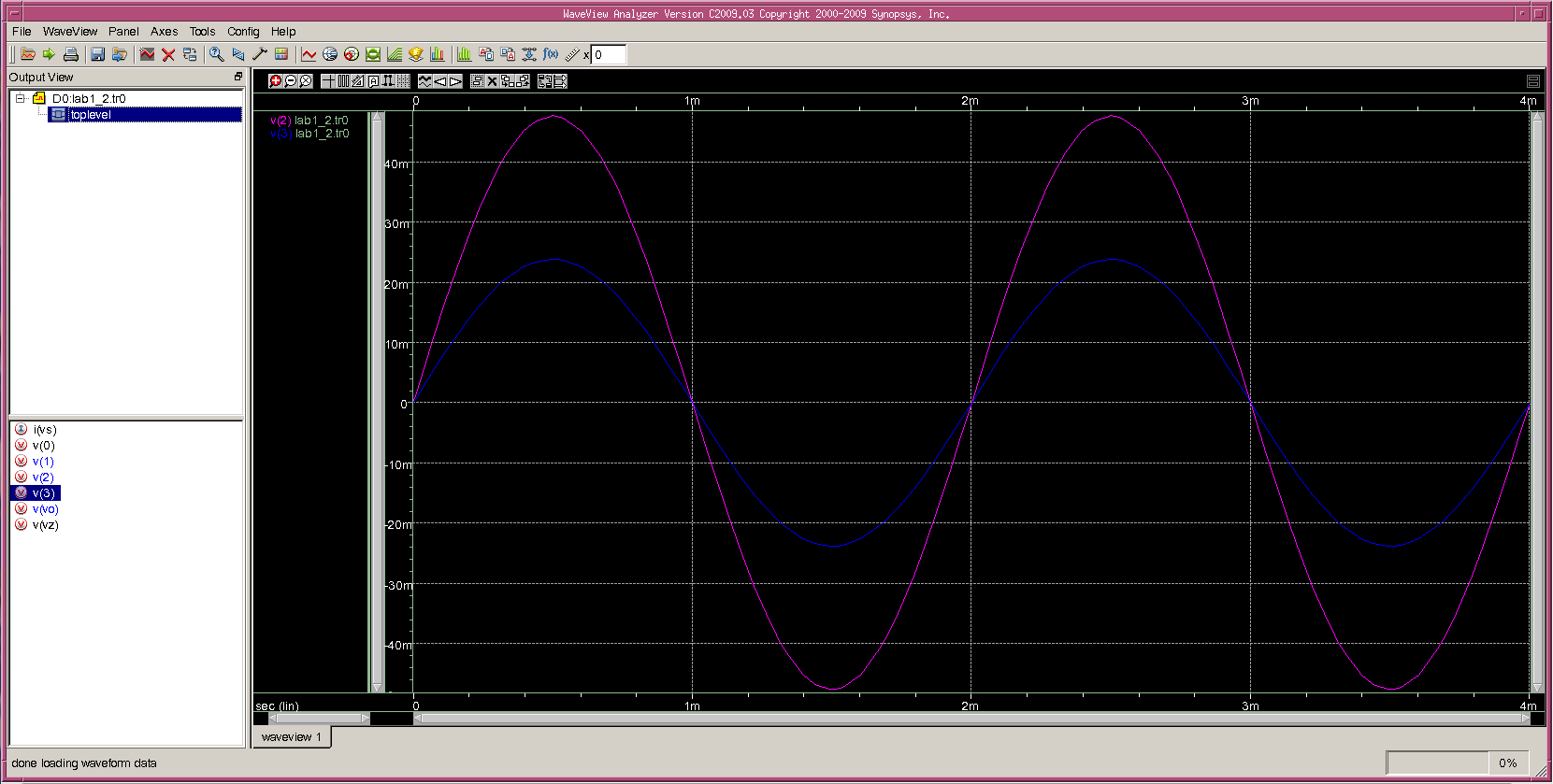
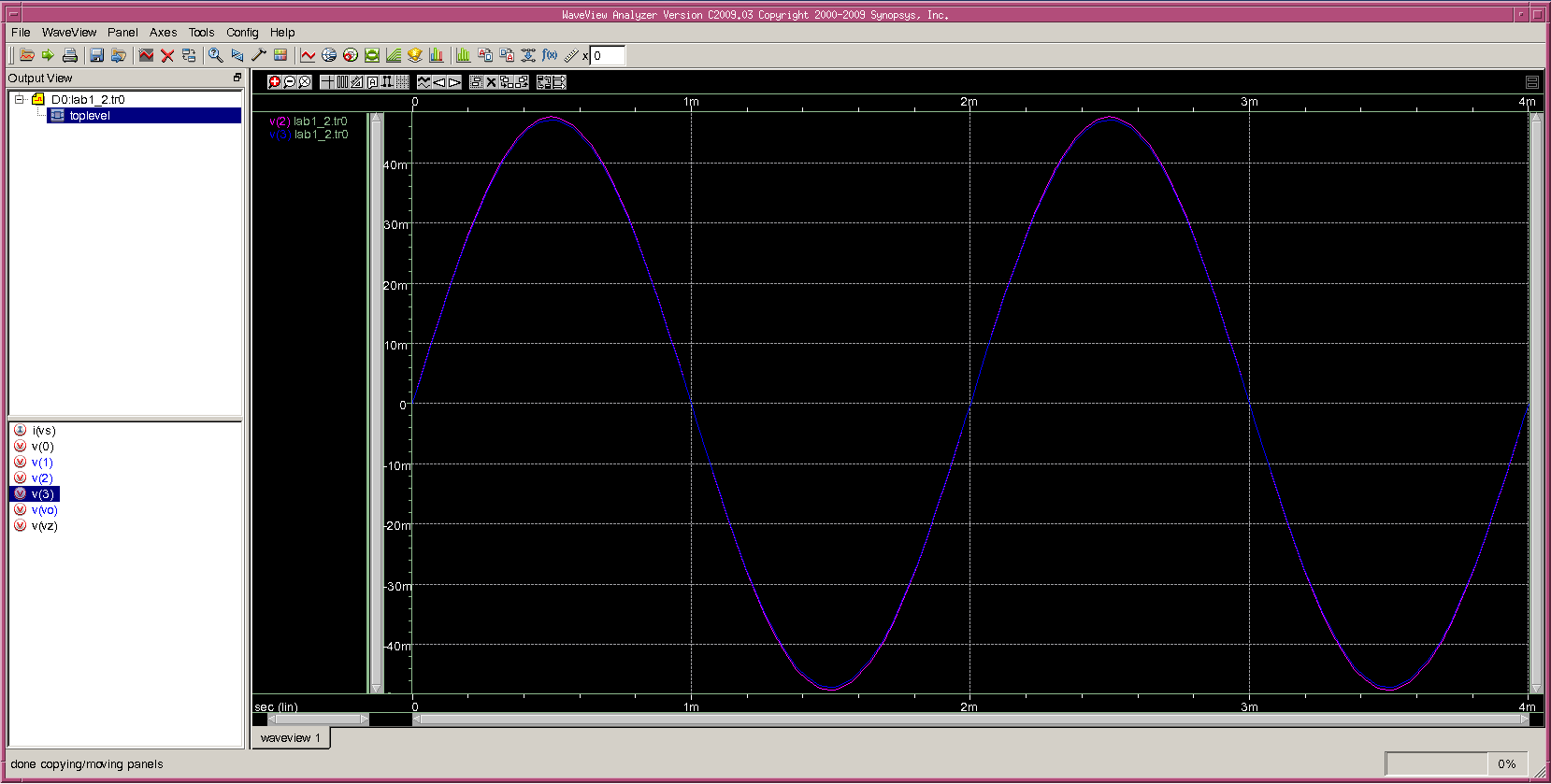
tstop=4ms

1. 

Amplitude of output signal: 2.4V~gain of 48.

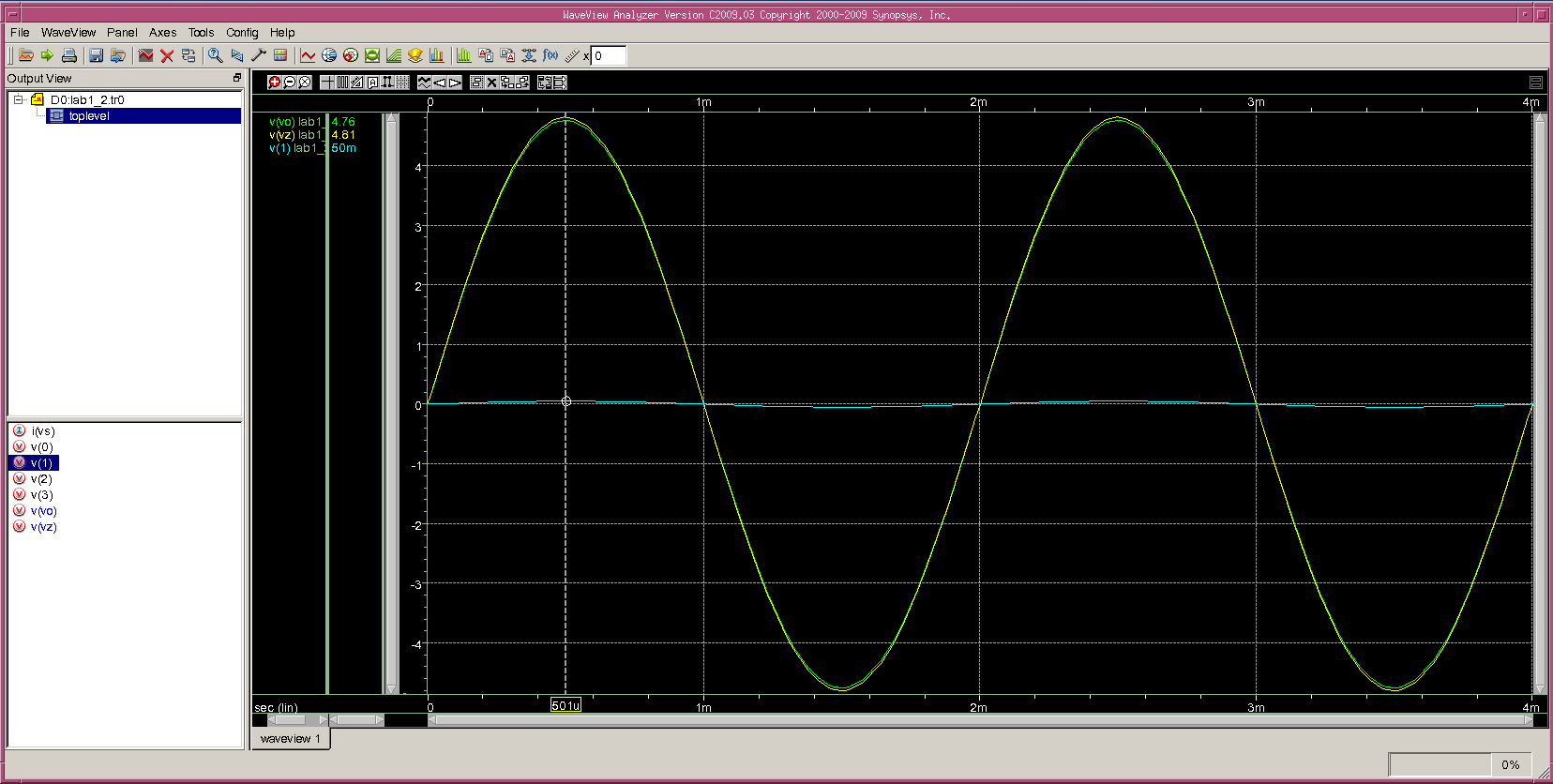
1. 

Amplitude of output signal: 4.76V~gain of 95.2

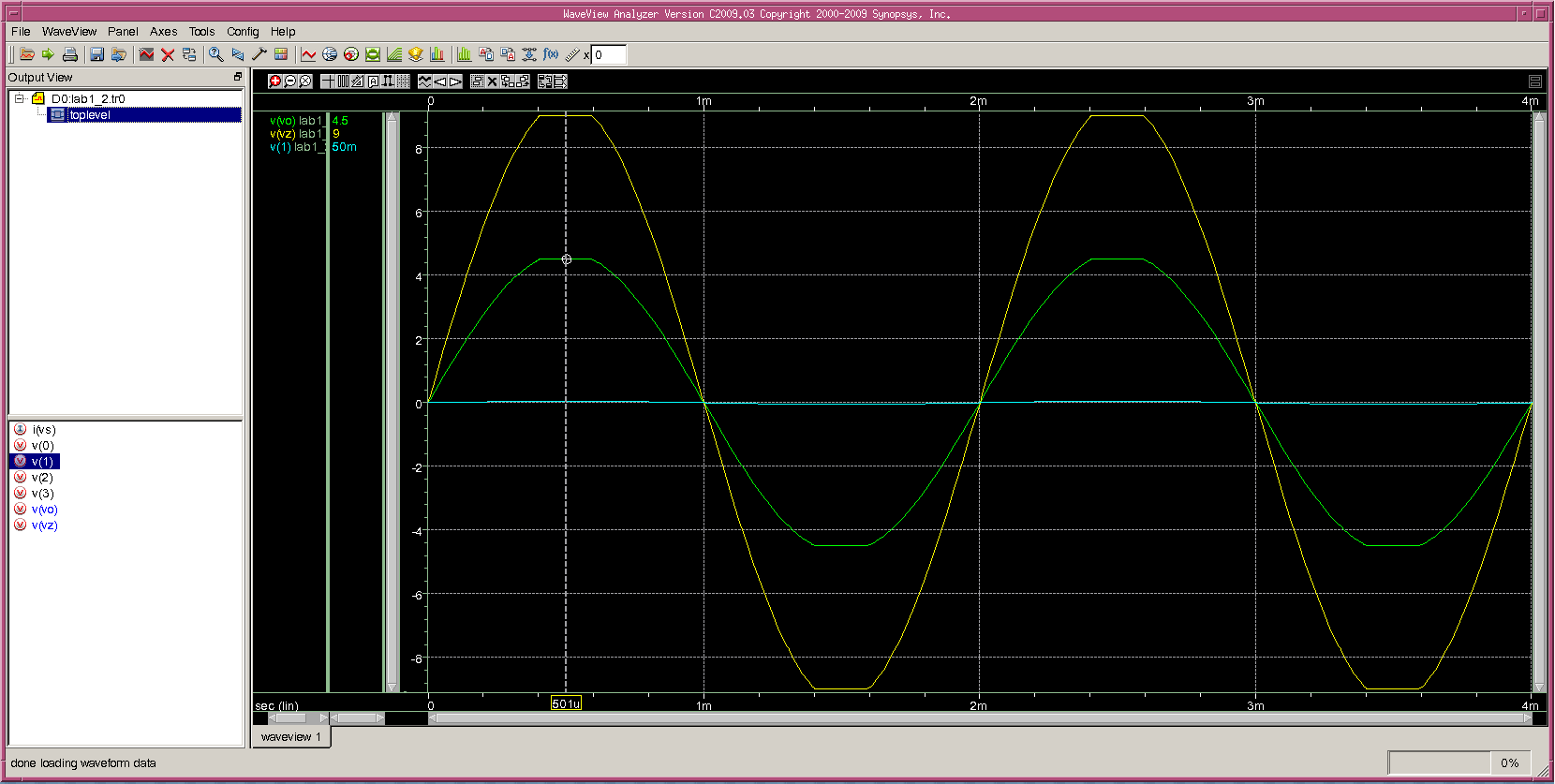
1. 
2. 

As can be seen, Increasing Ao definitely forces the input nodes of the op-amp closer together.



1. 1/2
2. 1
3. 101k.
4. ½
5. 1/1.01
6. 

Vo amplitude: 4.76. Vz amplitude:4.81. Vz/Vo~1.01. Vz/Vs~96.2.

1. 

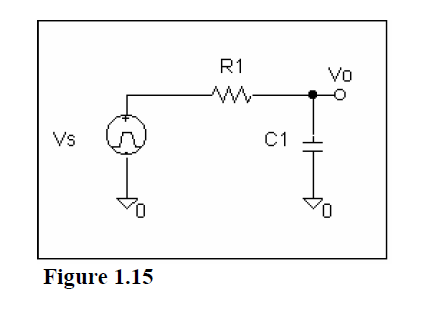
We can see that clipping occurs. This is because the gain of 190.48 would put Vz at 9.524V, but the max value it can reach is 9V.

**Exercise 3)**

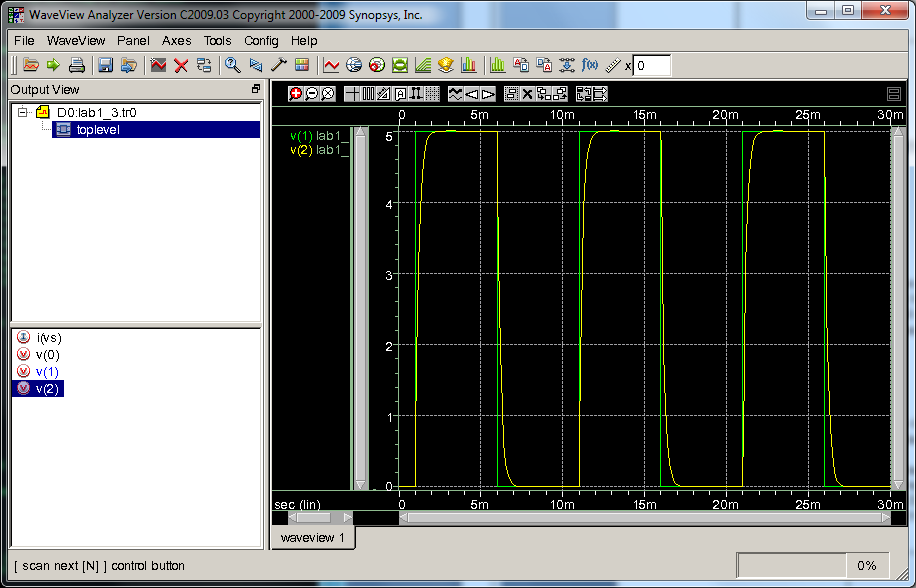
1. Use a transient (.TRAN) simulation on the circuit in figure 1.15 to plot Vo vs. Vs. Vs is a pulse generating source that alters between 0v and 5v. The source should have a 1ms delay, 5ms pulse width, 10ms period, and a rise and fall time of 1ps. Using R1=2k and C1=.1u, plot Vo vs. Vs for a tstep of 1u and the following transient simulation times:
2. 30ms
3. 300ms
4. .3ms

Show all plots in your report.

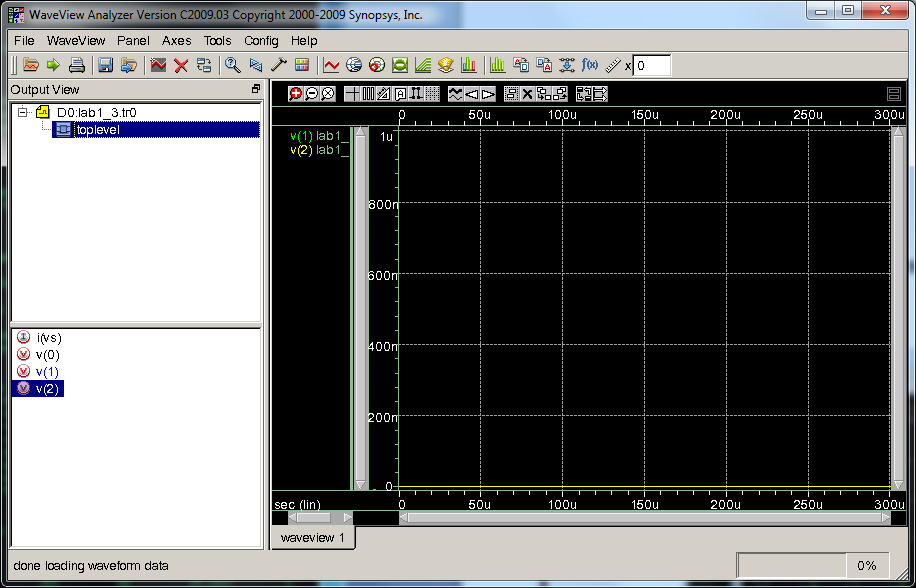
1. Do the results differ when using three different simulation times? Why is it important to make an educated decision when choosing a simulation time for your simulation?
2. The time constant of a first order system refers to the time it takes the system to reach within 1/e of its final value when the input is a step (Vout=Vfinal\*[1-e-1]). What is the time constant of this circuit? Verify this value with HSPICE by adding a curser to the wave viewer and finding the time it takes for the output to reach 63% of its final value. (You may need to zoom in the x-axis, time, to see this value.)



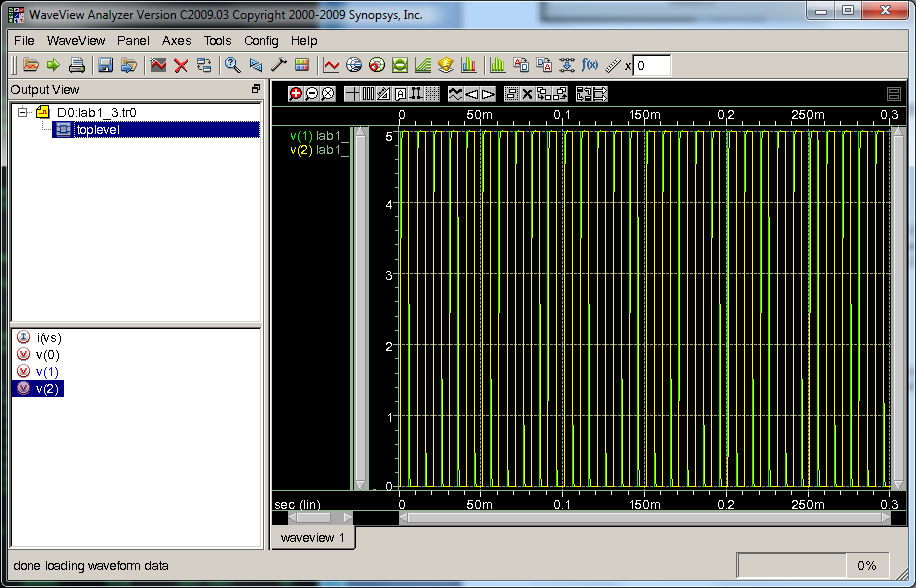
The results differ when using the three simulation times. You may not see what you are looking for if you don’t make an educated guess on simulation time. See next page for plots and answers to part C).



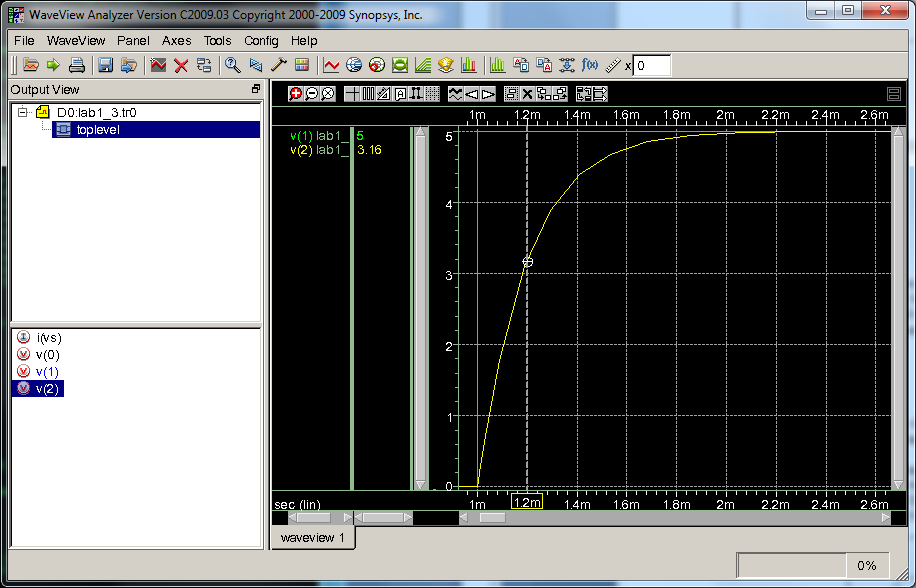
1)

****

3)

****

2)

****

Trise

Time constant = R\*C = .2ms. This can be seen in the plot Trise since the output rises to 63% of 5V (3.16V) from 1ms to 1.2ms.

**Exercise 4)**

1. Using the schematic in figure 1.15, peform an .AC analysis to plot a frequency sweep of Vo with 100 points per decade. Replace Vs with an ac source with a magnitude of 1V. Be sure to make the x-axis logarithmic in your plots.
2. Let R1=1k and C1=100p. Sweep from 10Hz-10kHz
3. Let R1=100k and C1=100n. Sweep from 10Hz-10GHz
4. Why did both of these sweeps fail to show a valid .AC sweep?
5. Let R1=100 and Cl=1p. Sweep from 10Hz=10GHz. What is the problem with this sweep?
6. One can see that choosing the correct frequency range optimizes the results. One common error ee348L students make is submitting poor plots. An original sweep from ‘DC to daylight’ can be a good way to get an idea of what frequency range is appropriate to sweep; however, this original plot should not be submitted. Find the -3db frequency of the circuit in Figure 1.15 from part A, number 1. (remember, 2\*π\*f-3db=w-3db). Run another ac sweep that sweeps two decades before and two decades after the -3db frequency. Be sure to make the x-axis logarithmic (right click on the scale in WaveView Analyzer).
7. What should be the magnitude of the value of Vo at the -3db frequency? Using the plot from part B, add a curser at the -3db frequency.

Include all plots in your lab report.

A



1)



2)

1. The first plot does not sweep long enough to capture the -3db. The second plot does not start early enough to capture the -3db.



1. This plot begins at way too early of a frequency. 90% of the plot is wasted on frequencies that are not of interest.

f-3db=1.59 MHz.

Vo should be .707 at f-3db.

